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EXAMINER	
FLOURNOY, HORACE L	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,277	SPENCER, ANDREW M.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,11,15,16,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,11,15,16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed 28 August 2006. Claims 1-8,10,11,15,16,18 and 19 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not entirely persuasive, as will be discussed in more detail below, even in light of the instant amendments. Accordingly, this action has been made NON-FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10,11,15,16,18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by **Bruce et al. (U.S. Patent No. 6,000,006 hereafter referred to as Bruce)** with MPCD (Microsoft Computer Dictionary) offered as extrinsic evidence.

With respect to **independent claim 10,**

> *"A method of providing access to stored data, the method comprising receiving a read command that comprises a read address;* **[Bruce discloses in column 2, lines 12-18, "When a one is encountered when reading re-map table 15, a separate address re-map table (not shown) is consulted to find the physical**

address. This address re-map table is typically stored in the last block of each flash device."] *determining whether data from the read address is buffered in a volatile read buffer; retrieving data from a location in a nonvolatile memory array associated with the read address if the data is not buffered, and buffering the retrieved data in the volatile read buffer;* **[Bruce discloses in column 4, lines 5-8, "The cache index identifies a location in the cache of the data for the logical address. Thus each entry identifies the location in cache for the data or the location in the flash-memory devices." See column 3, line 66-column 4, line 8.]** *responding to the read command with data from the volatile read buffers if the data is buffered;* **[disclosed, e.g. in the abstract, "When the cache valid bit is set, the data is read or written to a line in the cache pointed to by the cache index. A separate cache tag RAM is not needed. When the cache valid bit is cleared, the data is read from the flash memory block pointed to by the PBA."]** *detecting a pending power-down; storing in nonvolatile memory the read address for data buffered in the volatile read buffer;* **[disclosed, e.g. in column 6, lines 43-50]** *and* ~~*: preserving during an absence of electrical power information indicative of data in one or more read buffers; and*~~ *restoring the data to the* ~~*one or more read buffers*~~ *volatile read buffer when power returns.* ~~*wherein said preserving comprises: detecting a pending power-down; for each of the one or more read buffers, storing in nonvolatile memory a starting address of memory blocks that have been recently accessed."*~~ **[disclosed, e.g. in column 11, lines 5-18]**

With respect to **independent claim 15**,

"A digital device that comprises: a memory having a buffered memory interface with one or more read buffers **[Bruce discloses in column 2 line 65 - column 3, line 3, "Each entry in the plurality of entries has a physical-block-address field that contains a physical block address of a block in an array of flash-memory devices. Each flash-memory device contains non-volatile storage cells that retain data when a power supply is no longer applied to the flash-memory device."]** *and a processor coupled to the memory device and configured to retrieve stored information from the memory* **[See FIG. 4: "Host Requests" See column 6, lines 12-15]** *wherein the processor causes the memory to receive a power down command before electrical power is removed from the memory,* **[disclosed, e.g. in column 6, lines 43-50]** *and wherein the buffered memory interface responsively stores in a nonvolatile memory ~~information that represents~~ one or more addresses ~~within the memory~~ of memory locations that have been recently accessed."* **[Bruce discloses in column 13, lines 31-34, "A cache of the re-map table can be used rather than a full table when the access times for various blocks can vary. Rather than storing all entries for all flash blocks in RAM, only the most-recently-used entries can be stored." See also column 12, lines 44-50.]**

With respect to **claim 11,**

"The method of claim 10, wherein said restoring comprises ~~for each of the on or more read buffers~~: accessing the nonvolatile memory to retrieve the ~~starting~~ read address associated with the read buffer; and filling the read buffer with data from

a memory array, beginning with data associated with the ~~starting~~ read address. **[disclosed, e.g. in column 11, lines 5-18]**

With respect to **claim 16**,

"The device of claim 15, wherein the memory interface is further configured to reload the one or more read buffers with data in accordance with information from the nonvolatile memory when power returns" **[disclosed, e.g. in column 11, lines 5-18]**

With respect to **claim 18**,

"The device of claim 15, wherein the one or more read buffers comprise: a plurality of read buffers each associated with a different region of the memory **["cache index field" disclosed in column 4, lines 1-8]** *and configured to buffer only data for read operations on an associated region."* **[disclosed in column 3, line 66 –column 4, line 8]**

With respect to **claim 19**,

"The device of claim 18, wherein the memory interface further comprises: an interface control module that is configured to receive read commands specifying a memory address, wherein the interface control module is coupled to a nonvolatile memory array to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands; **[disclosed in the rejection to independent claim 7 below]** *and wherein the memory further comprises: an error correction code (ECC) decoder coupled*

between the nonvolatile memory array and the one or more read buffers."

[disclosed, e.g. in column 10, lines 16-28]

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being obvious over Bruce et al. (U.S. Patent No. 6,000,006 hereafter referred to as Bruce) in view of Tsunoda et al. (U.S. PG Publication No. 2003/0028733 hereafter referred to as Tsunoda).

- With respect to independent **claims 1 and 7,** *Bruce* teaches the following limitations:

Independent claim 1:

"An integrated memory device that comprises: a nonvolatile memory array; and a nonvolatile buffered memory interface integrated on a substrate with said nonvolatile memory array, **[Bruce discloses in column 2 line 65 - column 3, line 3, "Each entry in the plurality of entries has a physical-block-address field that contains a physical block address of a block in an array of flash-memory devices. Each flash-memory device contains non-volatile storage cells that retain data when a power supply is no longer applied to the flash-memory device."]** *wherein the memory interface comprises: one or more volatile buffers configured to buffer data for read operations directed to the integrated memory device;* **[see FIG. 4, element 22 and column 6, lines 12-25]** *and a table memory configured to ~~indicate one or more~~* identify *addresses within the nonvolatile memory array that have been recently accessed."* **[Bruce discloses in column 13, lines 31-34, "A cache of the re-map table can be used rather than a full table when the access times for various blocks can vary. Rather than storing all entries for all flash blocks in RAM, only the most-recently-used entries can be stored." See also column 12, lines 44-50.]**

Independent claim 7:

"An integrated memory device that comprises: a nonvolatile memory array: and a nonvolatile buffered memory interface integrated on a substrate with said nonvolatile memory array, **[Bruce discloses in column 2 line 65 - column 3,**

line 3, **"Each entry in the plurality of entries has a physical-block-address field that contains a physical block address of a block in an array of flash-memory devices. Each flash-memory device contains non-volatile storage cells that retain data when a power supply is no longer applied to the flash-memory device."]** *wherein the memory interface comprises: one or more volatile buffers configured to buffer data for read ~~operations~~ commands directed to the integrated memory device;* **[see FIG. 4, element 22 and column 6, lines 12-25]** *~~and~~ a table memory configured to ~~indicate one or more~~ identify nonvolatile memory addresses associated with data buffered in the one or more volatile buffers;* **[Bruce discloses in column 13, lines 31-34, "A cache of the re-map table can be used rather than a full table when the access times for various blocks can vary. Rather than storing all entries for all flash blocks in RAM, only the most-recently-used entries can be stored." See also column 12, lines 44-50.]** *and ~~wherein the memory interface further comprises:~~ an interface control module that is configured to receive read commands specifying a memory address, wherein the interface control module is coupled to the memory array to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands,* **[Bruce discloses in column 2, lines 12-18, "When a one is encountered when reading re-map table 15, a separate address re-map table (not shown) is consulted to find the physical address. This address re-map table is typically stored in the last block of each flash device."]** *wherein the interface control module is further configured to update the table memory in response to the read*

commands." **[See column 12, lines 44-50. Bruce teaches "wear-leveling" which updates the table memory in response to the read commands.]**

- *Bruce*, however, does not disclose *expressly* the limitation of *"integrated on a substrate"* as disclosed on line 3 of independent claim 1 and line 3 of independent claim 7.
- *Tsunoda* teaches in paragraph [0124], lines 2-5, "For example, the apparatus may be a LSI, in which memory chips and a control chip are sealed in one package, or all the functions may be housed on one semiconductor chip."
- *Bruce* and *Tsunoda* are analogous art because they are from the same field of endeavor, that being non-volatile and volatile memory devices.
- At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate all elements sited above in Bruce, on a substrate, as outlined in Tsunoda.
- The *motivation* for doing so would have been obvious based on the teaching of the Tsunoda in paragraph [0124], lines 2-5. Furthermore, integrating a group of elements that form a functional device on a substrate, is well known to persons of ordinary skill in the art.
- Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Bruce and Tsunoda before him/her to combine Tsunoda and Bruce for the benefit of having the elements outlined above in independent claims 1 and 7 integrated on a substrate.

With respect to **claim 2**,

> *"The device of claim 1, wherein the table memory is volatile,* **[See FIG. 4 and all associated text within specification]** *and wherein the memory interface is configured to preserve contents of the table memory in nonvolatile memory during absences of electrical power"* **[Bruce discloses in column 2 line 65 - column 3, line 3, "Each entry in the plurality of entries has a physical-block-address field that contains a physical block address of a block in an array of flash-memory devices. Each flash-memory device contains non-volatile storage cells that retain data when a power supply is no longer applied to the flash-memory device."]**

With respect to **claim 3**,

> *"The device of claim 2, wherein the memory interface is further configured to restore the contents of table memory from the nonvolatile memory when electrical power returns"* **[disclosed, e.g. in column 11, lines 5-18]**

With respect to **claim 4**,

> *"The device of claim 1, wherein when electrical power returns, the memory interface is further configured to restore the one or more volatile buffers to a state preceding the absence of electrical power"* **[disclosed, e.g. in column 11, lines 5-18]**

With respect to **claim 5,**

"The device of claim 1, wherein the one or more volatile buffers comprise: a plurality of read buffers each associated with a different region of the memory array **["cache index field" disclosed in column 4, lines 1-8]** *and configured to buffer only a subset of data in the associated region for read operations on that ~~the associated~~ region"* **[disclosed in column 3, line 66 –column 4, line 8]**

With respect to **claim 6**,

"The device of claim 1, wherein the memory array comprises magnetic random access memory (MRAM) cells" **[The use of magnetic random access memory for a memory array is well known to persons of ordinary skill in the art]**

With respect to **claim 8**,

"The device of claim 7, further comprising: an error correction code (ECC) decoder coupled between the memory array and the one or more volatile buffers" **[disclosed, e.g. in column 10, lines 16-28]**

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Response to Arguments

Applicant's arguments with respect to **claims 1-8,10,11,15,16,18 and 19** have been considered but are moot in view of the new ground(s) of rejection. New grounds of rejection necessitated by applicant's amendments to the claims.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status

information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy

Patent Examiner
Art unit: 2189

Reginald G. Bragdon

Supervisory Patent Examiner
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